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10/083,395	02/27/2002	Masahide Tokuda	520.41288X00	7372

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EXAMINER	
BATTAGLIA, MICHAEL V	
ART UNIT	**PAPER NUMBER**
2652	3

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,395	TOKUDA ET AL.	
	Examiner	Art Unit	
	Michael V Battaglia	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) ~~1-20~~ is/are allowed.

6)☒ Claim(s) *1,2 and 11-20* is/are rejected.

7)☒ Claim(s) 3-10 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figure 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 1, 7, 8, 13, 14 and 16 and therefore 2-6, 9-12, 15 and 17-20 are objected to because of the following informalities.

a. On line 16 of claim 1, line 22 of claim 14, and line 27 of claim 16, removal of "letting" is suggested.

b. On lines 33-34 of claim 1 and lines 39-40 of claim 14, replacing "the semiconductor element" with -the optical device— is suggested to avoid improper antecedent basis issues.

c. In reference to line 3 of claims 7 and 8, correction of "therebelow", not found in *The American Heritage Dictionary* used by the US Patent Office. Correction, is suggested.

d. On line 4 of claim 7, replacing "one" with -on— is suggested.

e. On line 5 of claim 13, replacing "layer" with -electrode— is suggested.

f. On line 4 of claim 16, inserting -an- in "and optical" is suggested.

g. On line 7 of claim 16, replacing "at a least" with -at least a— is suggested.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Ozawa (US 6,474,531).

In regard to claim 1, Ozawa discloses a method of mounting an optical device comprising the steps of: preparing a substrate (Figs. 3-4, element 31) in which at least a first electrode (Figs. 3-4, element 32) and a second electrode (Figs. 3-4, element 33) are disposed and an optical device (Figs. 2 and 4, element 20) in which a third electrode (Figs. 2 and 4, element 2A) and a fourth electrode (Figs. 2 and 4, element 2B) are disposed corresponding to the first electrode and the second electrode respectively, in which surfaces for mounting the third electrode and the fourth electrode of the optical device have a first height (ah1) and a second height (ah2) from one surface of the optical device on the side opposite to the surface for mounting the third electrode and the fourth electrode, respectively, where ah1>ah2, each of the first electrode and the second electrode has at least a solder-underlying region and solder (Figs. 3-4, elements 4A and 4B) on the solder-underlying region, and the solder-underlying region area of the first electrode is aS1, the solder-underlying region area of the second electrode is aS2, the third electrode area is aS3, the fourth electrode area is aS4, the volume of a solder disposed on the solder-underlying region of the first electrode is v1, and the volume of a solder disposed on the solder-underlying region of the second electrode is v2, v1 is not equal to v2 (Figs. 3-4), and each of the values of ah1, v1, aS1, ah2, v2 and aS2 is set so that the height of the first electrode and the second electrode from the surface of the solder-underlying region to the opposing surface of the optical device is a height in proportion to ah1+v1/aS1 or ah2+v2/aS2 after the solder has been melted; and positioning the substrate and the optical device so that the third electrode of the optical device is disposed on the first electrode of the substrate and the fourth electrode of the optical device is disposed on the second electrode of the substrate, melting the solder and soldering the semiconductor element to the substrate (Fig.

4B). The regions of the first and second electrodes underneath the solder and in contact with the solder are interpreted as solder underlying regions. It is noted that any length can be interpreted as being in proportion to another length if the proportion is not specified.

In regard to claim 2, Ozawa discloses that the volume (v1, v2) of the solder formed corresponding to each of the first electrode and the second electrode disposed on the substrate is prepared such that the value (v1/aS1, v2/aS2) obtained by dividing the volume (v1, v2) by each of the areas (aS1, aS2) of the solder-underlying region of the first electrode and the second electrode on the substrate has a relation of v2/aS2 > v1/aS1 (Figs. 1 and 4B).

In regard to claim 11, Ozawa discloses that the solder is an alloy of gold (Au) and tin (Sn) (Col. 4, lines 64-66).

In regard to claim 12, Ozawa discloses that the substrate is a silicon substrate (Col. 5, lines 39-43).

In regard to claim 13, Ozawa specifies that the area of the solder-underlying region of the first electrode is substantially identical with that of the third electrode, and the area of the solder-underlying region of the second layer is substantially identical with that of the fourth electrode (Figs. 4A and 4B).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al (hereafter Kitamura) in view of Ozawa.

In regard to claim 14, Kitamura discloses an optical head device comprising: a light source (Fig. 1, element 3) for irradiating a disk substrate with light to conduct at least one of writing and reading of information and a driving circuit (Fig. 1, element 11) for driving the light source to output light. Kitamura does not disclose the structural limitations implied by the light source mounting method of claim 14.

Ozawa discloses a light source (Figs. 2 and 4, element 20) that is mounted by a mounting method having the following implied structural limitations implied: a substrate (Figs. 3-4, element 31) in which at least a first electrode (Figs. 3-4, element 32) and a second electrode (Figs. 3-4, element 33) are disposed and an optical device (Figs. 2 and 4, element 20) in which a third electrode (Figs. 2 and 4, element 2A) and a fourth electrode (Figs. 2 and 4, element 2B) are disposed corresponding to the first electrode and the second electrode respectively, in which surfaces for mounting the third electrode and the fourth electrode of the optical device have a first height (ah1) and a second height (ah2) from one surface of the optical device on the side opposite to the surface for mounting the third electrode and the fourth electrode, respectively, where ah1>ah2, each of the first electrode and the second electrode has at least a solder-underlying region and solder (Figs. 3-4, elements 4A and 4B) on the solder-underlying region, and the solder-underlying region area of the first electrode is aS1, the solder-underlying region area of the second electrode is aS2, the third electrode area is aS3, the fourth electrode area is aS4, the volume of a solder disposed on the solder-underlying region of the first electrode is v1, and the volume of a solder disposed on the solder-underlying region of the second electrode is

v2, v1 is not equal to v2 (Figs. 3-4), and each of the values of ah1, v1, aS1, ah2, v2 and aS2 is set so that the height of the first electrode and the second electrode from the surface of the solder-underlying region to the opposing surface of the optical device is a height in proportion with ah1+v1/aS1 or ah2+v2/aS2 after the solder has been melted, and the substrate and the optical device positioned so that the third electrode of the optical device is disposed on the first electrode of the substrate and the fourth electrode of the optical device is disposed on the second electrode of the substrate, the semiconductor element is soldered to the substrate (Fig. 4B). The regions of the first and second electrodes underneath the solder and in contact with the solder are interpreted as solder underlying regions. It is noted that any length can be interpreted as being in proportion to another length if the proportion is not specified. Ozawa discloses the mounting method with the implied structural limitations prevents short circuit failure, beam shape change, and laser beam intensity decrease (Col. 8, lines 13-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate into optical head of Kitamura the structural limitations implied by the light source mounting method of Ozawa, the motivation being to prevent short circuit failure, beam shape change, and laser beam intensity decrease caused when mounting the light source.

In regard to claim 15, Kitamura discloses that the light source has a constitution in which plural semiconductor laser devices (Figs. 1 and 8, element 3) are mounted on a predetermined substrate (Fig. 1, element 10). The plural semiconductor laser devices are mounted by the method of Ozawa and have the structure implied by the method of Ozawa including, at least one semiconductor laser device having plural electrodes connected

electrically to the plural electrodes on the substrate which are formed at positions corresponding to the surface of the substrate and at different levels (Fig. 4B).

In regard to claim 16, Kitamura discloses that the light source includes plural semiconductor laser devices (Figs. 1 and, element 3), an optical detector for automatic focusing detection and an optical detector for tracking detection mounted monolithically on a predetermined substrate (Fig. 1, elements 13a-h; Col. 9, lines 36-40; and Col. 11, lines 26-40), and in which optical paths from the optical source to the disk substrate passing through the light source, a beam splitter (Fig. 1, element 6) and an objective lens (Fig. 1, element 5) is made into a single constitution (Fig. 1, element 2). The plural semiconductor laser devices are mounted by the method of Ozawa and include the structural limitations implied thereby as described in the rejection of claim 14 above, which includes at least one semiconductor laser device in which at least a first electrode and a second electrode connected electrically to the plural electrodes on the substrate are formed at the height different from each other from one surface of the substrate of the semiconductor laser device (Fig. 4B).

In regard to claim 17, Kitamura discloses that the substrate is a semiconductor substrate (Col. 9, lines 39-40).

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura in view of Ozawa as applied to claim 16 above, and further in view of Nishi (US 6,700,842).

Kitamura the light source includes plural semiconductor laser devices (Figs. 1 and 8, element 3) and optical detectors for automatic focusing detection and optical detectors for tracking detection (Fig. 1, elements 13a-h) mounted monolithically on a predetermined substrate (Fig. 1, element 10 and Col. 9, lines 36-40). Kitamura further discloses an

arithmetic circuit (Fig. 1, element 12) that operates on the signals obtained from the optical detectors. Kitamura does not disclose that amplifiers for amplifying signals from both of the detectors are also mounted monolithically on the predetermined substrate.

Nishi discloses an amplifier, formed on the same substrate on which optical detectors are formed, that converts a current signal to a voltage signal that is operated on by an arithmetic circuit to produce focus and tracking detection signals (Col. 14, lines 22-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to also mount amplifiers on the substrate of Kitamura as suggested by Nishi, the motivation being to amplify the signals from the optical detectors and produce a signal usable by the arithmetic circuit for focusing and tracking detection.

9. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura in view of Ozawa as applied to claim 16 above, and further in view of Saitoh et al (hereafter Saitoh) (US 6,747,939).

In regard to claim 19, Kitamura does not disclose that a material layer having a high thermal conductivity is disposed between the substrate and the semiconductor laser device.

Saitoh in view of Ozawa discloses disposing a material layer (Fig. 6, element 18) having a high thermal conductivity between a substrate (Fig. 6, element 8) and a semiconductor laser device (Fig. 6, element 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a material layer having a high thermal conductivity between the substrate and the semiconductor laser device in the optical head of Kitamura in view of Ozawa as suggested by Saitoh, the motivation being to dissipate heat generated by the semiconductor laser device.

In regard to claim 20, the material layer of Saitoh, added to the optical head of Kitamura in view of Ozawa for claim 19 above and disposed between the substrate and the semiconductor laser device would also be capable of relaxing stresses caused by differences in heat expansion between the substrate and the semiconductor through heat dissipation.

Citation of Relevant Prior Art

10. Tada (US 5,668,822) discloses multiple semiconductor lasers mounted on a substrate (Fig. 1). Torii (JP 04-242939) discloses mounting of a semiconductor device by providing a plurality of electrodes of different heights (Fig. 1). Tanabe et al (US 6,725,230) discloses an optical device having a stepped surface with an electrode on each step that is soldered to a substrate using different amounts of solder to compensate for the height difference between the electrodes (Fig. 20). Yamamoto et al discloses an optical device having an electrode located on each of two steps having different heights that is mounted on a substrate having electrodes using different amounts of solder to account for the height difference (Fig. 29). Takase et al (US 6,028,011) discloses the volume and height of solder on an electrode (Fig. 5). Yamada et al (JP 09-223846) discloses an optical device having a stepped surface with an electrode on each step that is mounted to a substrate by soldering each electrode of the optical device to respective electrodes of the substrate (Fig. 3).

Allowable Subject Matter

11. Claims 3-10 would be allowable if rewritten to overcome the objections set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

None of the references of record alone or in combination disclose or suggest a method of mounting an optical device comprising the steps of: preparing a substrate in which at least a first electrode and a second electrode are disposed and an optical device in which a third electrode and a fourth electrode are disposed corresponding to the first electrode and the second electrode respectively, in which surfaces for mounting the third electrode and the fourth electrode of the optical device have a first height (ah1) and a second height (ah2) from one surface of the optical device on the side opposite to the surface for mounting the third electrode and the fourth electrode, respectively, where ah1>ah2, each of the first electrode and the second electrode has at least a solder-underlying region and solder on the solder-underlying region, and letting the solder-underlying region area of the first electrode is aS1, the solder-underlying region area of the second electrode is aS2, the third electrode area is aS3, the fourth electrode area is aS4, the volume of a solder disposed on the solder-underlying region of the first electrode is v1, and the volume of a solder disposed on the solder-underlying region of the second electrode is v2, v1 is not equal to v2, and each of the values of ah1, v1, aS1, ah2, v2 and aS2 is set so that the height of the first electrode and the second electrode from the surface of the solder-underlying region to the opposing surface of the optical device is a height in proportion to ah1+v1/aS1 or ah2+v2/aS2 after the solder has been melted; and positioning the substrate and the optical device so that the third electrode of the optical device is disposed on the first electrode of the substrate and the fourth electrode of the optical device is disposed on the second electrode of the substrate, melting the solder and soldering the optical device to the substrate as claimed in claim 1 **AND** wherein the **surface of the second electrode of the substrate that is in contact with and covered with the solder**

has a region of material having a nature of increasing the height of solder to higher than the initial height by the melting of the solder, and the area of the solder prepared for the second electrode is larger than the area of the solder-underlying region below the solder, in the preparation step as in claims 3 or 4 **OR** wherein the surface of the first electrode of the substrate that is in contact with and covered with the solder has a region of material having a nature of decreasing the height of solder to lower than the initial height by the melting of the solder, and the area of the solder prepared for the first electrode is formed smaller than the area of the solder-underlying region below the solder, in the preparation step as in claims 5 or 6 **OR** wherein the solder-underlying region has a solder underlying layer and a conductor layer disposed therebelow and has the solder layer one the solder underlying layer as in claims 7 or 8.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael V Battaglia whose telephone number is (703) 305-4534. The examiner can normally be reached on 5-4/9 Plan with 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael V. Battaglia

W. R. YOUNG
PRIMARY EXAMINER